Transversal Radio Frequency Filter Integrated Circuit (TRAFFIC)

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***Abstract*—TRAFFIC is a general-purpose, high-performance transversal filter monolithic microwave integrated circuit (MMIC) in silicon germanium (SiGe) for direct-throughput processing of RF signals in the microwave and millimeter wave spectrum. This technology is a central component necessary to advance the emerging class of systems that perform analog signal processing, with the promise of greatly reducing the SWaP of RF front-ends while providing broadband instantaneous reconfigurability and multi-function RF capability. This core technology is expected to accomplish a diverse set of tasks, including tunable RF front-end filtering, pre-linearization of signals for amplifier saturation compensation, and direct throughput matched filtering. These capabilities are critical for a number of EW and communications applications.**

Keywords—analog filter; silicon germanium; SiGe; monolithic microwave integrated circuit; MMIC; radio frequency integrated circuit; RFIC; reconfigurable

I. Introduction

Modern RF systems for DoD applications are facing two major design challenges: mission expansion with constrained SWaP and spectrum density. The first challenge has led to a substantial push in so-called converged systems; that is, RF systems that can perform a plurality of functions (radar, EW, communications) with a single set of reconfigurable hardware. Programs such as AFRL's REMAR (Reconfigurable Electronics for Multifunction Agile RF) and DARPA's CONCERTO (Converged Collaborative Elements for RF Task Operations) seek to address this collapse of mission functions into a single RF system [1]. The second challenge leads to a need for spectrum reuse. Programs such as DARPA SPAR (Signal Processing at RF) and needs defined by the NSC (National Spectrum Consortium) are calling for hardware advances that increase capacity within a single frequency band [2]. There has been previous work on analog finite impulse response (FIR) filters, but these systems were focused on reducing intersymbol interference (ISI) and improving channel equalization in ultra-high-throughput fiber-optic systems [3].

To address these concerns, Georgia Tech is developing an adaptive, analog FIR filter MMIC with integrated digital control in a commercial silicon-germanium (SiGe) process, which will enable direct RF processing of signals in a low-SWaP/low-latency RF front-end. This circuit provides a generalized, dynamically reconfigurable RF component that can realize, for example, tunable RF front-end filtering, pre-linearization of signals for amplifier saturation compensation (leading to more efficient power amplifier operating modes), and direct throughput matched filtering. These developments are a result of an on-going, three-year internal research and design effort between the Georgia Tech Research Institute and the Georgia Institute of Technology.

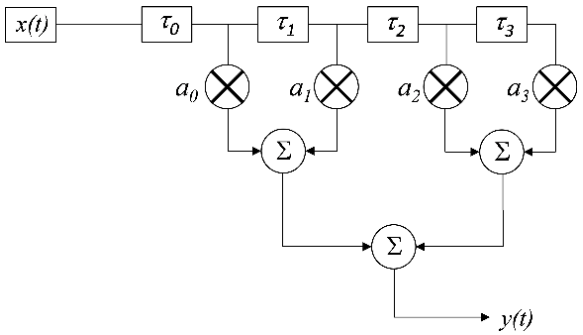
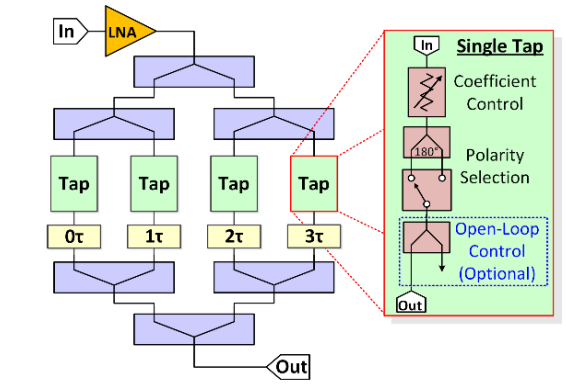


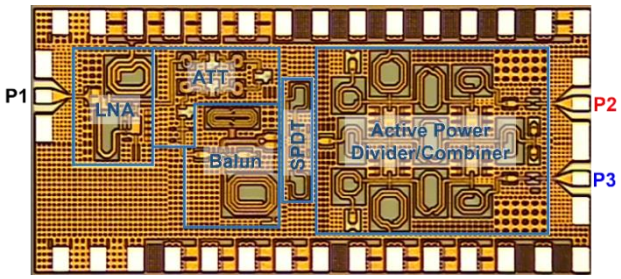
Fig. 1. Signal flow diagram of a general time-domain, 4-tap FIR filter.

II. System Description

Fig. 1 shows a signal flow diagram of a generalized FIR filter where the output of the filter is created as a superposition of delayed and weighted versions of the input. An infinite impulse response filter (IIR) can be realized with this architecture if delayed and weighted versions of the output are fed back into the input. TRAFFIC leverages this proven digital transversal design as the basis for an analog approach that consists of delay lines, linear amplifiers, power splitters, and multiplexers, implemented as a MMIC using GlobalFoundries 0.13μm BiCMOS8HP (GF-8HP) [4], a third-generation SiGe process providing *npn* SiGe heterojunction bipolar transistors (HBTs) with a peak f_t/f_{MAX} of approximately 200/265 GHz. These SiGe design platforms are ideally suited to combine high-performance RF/mm-wave and precision analog circuits with on-chip, high-speed digital interfaces, thereby allowing for system-on-chip solutions (SoC) to a wide variety of applications. Furthermore, SiGe HBTs exhibit superior $1/f$ noise properties compared to CMOS and III-V devices, excellent performance across wide temperature ranges (from 70 mK to 600 K), and are highly tolerant to multi-Mrad total ionizing dose exposures [5] – [8], allowing these technologies to operate reliably in extreme environments.



(a)



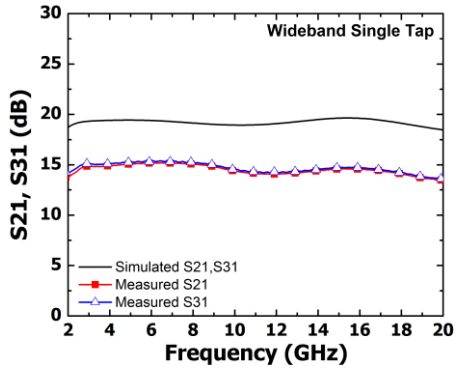
(b)

Fig. 2. (a) Block diagram of the multi-tap MMIC module and (b) die photomicrograph of the fabricated wideband single tap with an integrated LNA at the input (P1). Port 2 (P2) is the open-loop control port and port 3 (P3) is the FIR summed port. The chip dimensions are 2.24 mm × 1.06 mm.

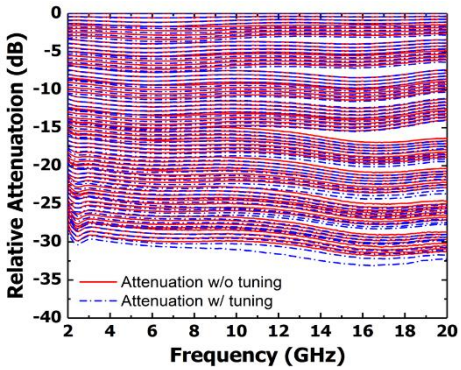
The block diagram for the TRAFFIC multi-tap MMIC module is shown in Fig. 2(a). Each 4-tap module consists of a low-noise amplifier (LNA), four single taps, and fixed true-time delay (TTD) elements to provide Nyquist sampling at the highest frequency of operation (i.e., inter-tap delay (τ) of 20 ps for a theoretical maximum operating frequency of 25 GHz). Each single tap provides coefficient control (variable gain or attenuation stage) and polarity selection (wideband balun + SPDT switch), thereby providing both positive and negative tap weights. An optional power divider stage at the tap output allows for active interrogation of individual taps while monitoring the summed FIR output. A die photomicrograph of the fabricated wideband single-tap MMIC is shown in Fig. 2(b). The dimensions of the chip are 2.24 mm × 1.06 mm.

III. Technical Results

All of the individual components of the single-tap MMIC have been designed and verified, and their integration into a single tap has been completed. As shown in Fig. 3(a), the single tap exhibits a flat gain response (13.5 – 15.2 dB) across all attenuation settings. A discrepancy is seen between Cadence Virtuoso simulations and laboratory measurements, where a fixed ~4 dB reduction from simulation is present across the entire frequency range. This shift is attributed to discrepancies in the EM modeling of the layout during the design process. The relative attenuation is shown in Fig. 3(b), where the data has been normalized to the zero attenuation state. The 7-bit digital step attenuator provides up to 31.75 dB



(a)



(b)

Fig. 3. (a) Measured S_{21} and S_{31} and (b) relative attenuation for the integrated single-tap MMIC.

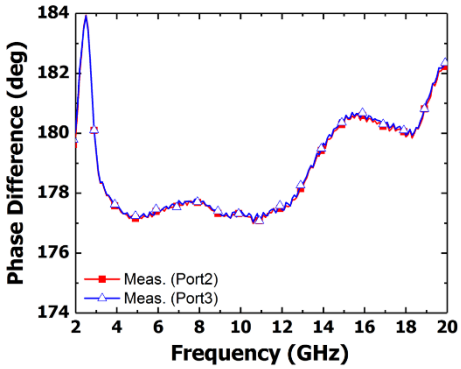


Fig. 4. Measured phase difference between positive and negative weights for the integrated single-tap MMIC.

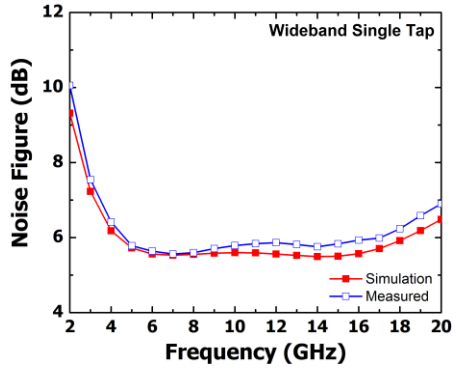
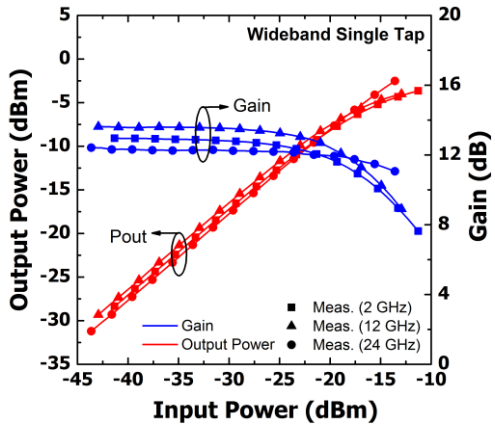


Fig. 5. Measured noise figure of the integrated single-tap MMIC.



(a)

Fig. 6. Measured output power and power gain of the integrated single-tap MMIC. Plots are overlaid for input frequencies of 2, 12, and 24 GHz.

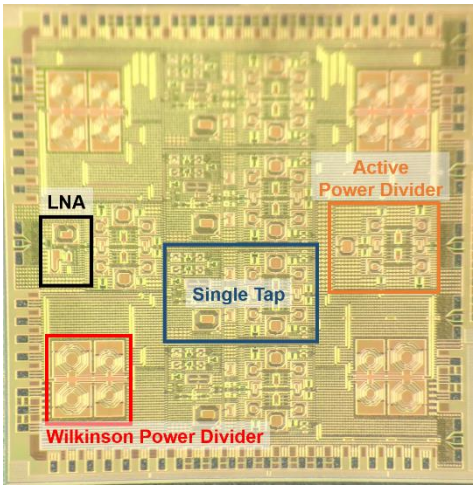


Fig. 7. Die photomicrograph of the fabricated 4-tap MMIC module, with sub-components highlighted for clarity. The chip dimensions are 3.84 mm × 3.98 mm.

of attenuation, with the least significant bit (0.25 dB) acting as a tuning bit to help achieve a flat-band response, particularly at higher frequencies. Fig. 4 shows the phase difference of the output signal, wherein the single tap exhibits minor phase mismatch (3 – 4°) across all polarity settings and thereby assures accurate control of positive and negative tap weights. To limit distortion of weak input signals, a target noise figure specification of 7 dB was set for the wideband single tap. As seen in Fig. 5, the single tap meets or exceeds this specification, with a noise figure of 5.8 dB at 10 GHz. Output power and power gain are shown in Fig. 6, where the single tap exhibits an input-referred compression point (IP_{1dB}) of approximately -21 dBm. While not shown for brevity, the single tap exhibits acceptable input and output return losses (>10 dB) across its entire operational bandwidth. In addition to the single tap chip, a completely integrated 4-tap MMIC design recently returned from fabrication and is awaiting characterization. A die photomicrograph of the fabricated 4-tap MMIC is shown in Fig. 7. The dimensions of the chip are 3.84 mm × 3.98 mm. Additional results for this final MMIC will be presented at the conference.

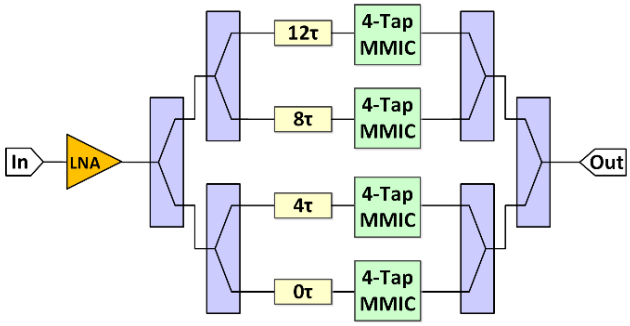


Fig. 8. Block diagram of a 16-tap FIR MMIC demonstrator utilizing four packaged 4-tap MMIC modules.

To increase the number of taps, multiple 4-tap blocks can be connected in parallel either at die level (e.g., as multi-chip modules) or at the PCB level. A block diagram of this modular, "many-tap" approach is shown in Fig. 8 for a 16-tap FIR MMIC demonstrator. This system architecture is similar to the integrated 4-tap MMIC in Fig. 2(b), except that each single tap is replaced with a 4-tap block and the time delay is scaled appropriately (i.e., $0\tau = 0$ ps for the first 4-tap block, $4\tau = 80$ ps for the second block, $8\tau = 160$ ps for the third block, and so forth). This parallel approach is functionally identical to the serial FIR topology in Fig. 1, but improves insertion loss due to reduced power splitting. Laboratory measurements of this FIR demonstrator are pending, but in order to test the multi-chip architecture, RF simulations were completed using the single-tap MMIC to model a 16-tap reconfigurable FIR filter across multiple configurations (low-pass, high-pass, band-pass, and band-stop). The simulated forward gain (S_{21}) for these different filter configurations are shown in Fig. 9. For all simulations, the inter-tap delay was set to 20 ps (i.e., Nyquist sampling at 25 GHz), the RF input power was set to -20 dBm, and the tap coefficients were optimized to minimize passband ripple. The 16-tap TRAFFIC filter responses are in agreement with ideal FIR theory, though out-of-band suppression is slightly degraded due to the finite attenuation provided by the 7-bit digital step attenuator in the single tap. It should be noted, however, that optimization techniques (e.g., gradient descent, recursive least squares, etc.) may improve the filter response as well as enable FIR algorithms for other RF processing applications. These results highlight the potential of TRAFFIC to create a dynamically tunable FIR for use as a highly adaptable RF front-end.

IV. Conclusions

TRAFFIC is a low-SWAP reconfigurable component for RF systems that will enable front-end direct processing of RF signals for frequency filtering, linearization, matched filtering, and isolation. This development will satisfy critical cross-domain DoD needs in multi-function spectrum-dense applications as well as in small form-factor applications (e.g., unmanned platforms and dismount) that were previously limited to platforms with larger weight/power budgets for digital systems.

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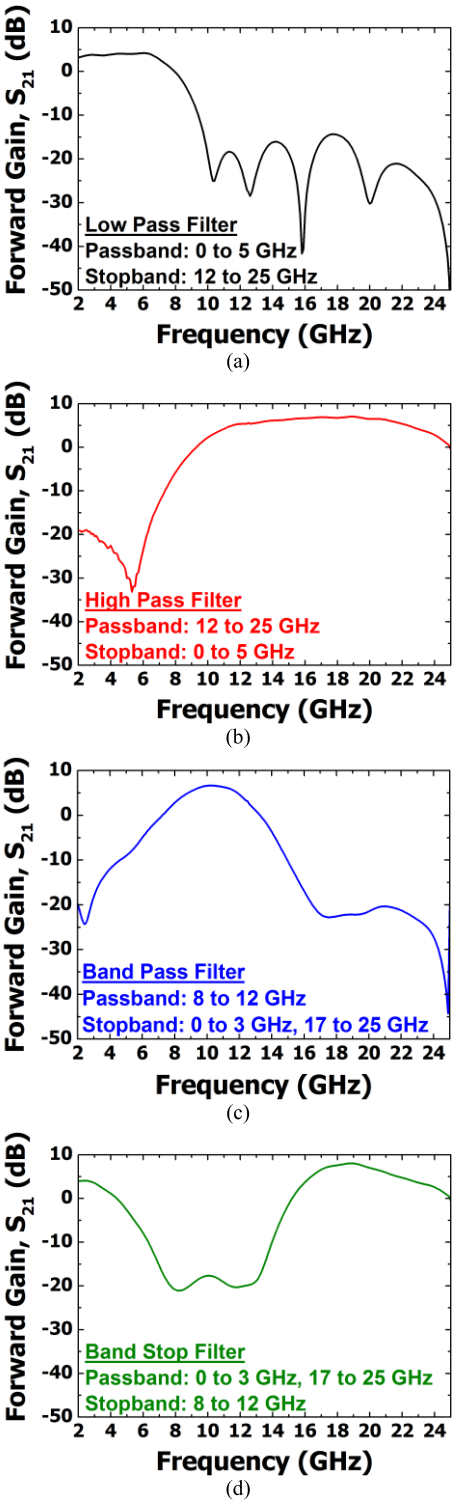

Fig. 9. Simulated forward gain (S_{21}) for a 16-tap TRAFFC reconfigurable filter configured as: (a) low pass filter, (b) high pass filter, (c) band pass filter, and (d) band stop filter. All tap coefficients were optimized to minimize passband ripple.